IN THE CLAIMS:

1. (Currently Amended) A semiconductor integrated circuit comprising:

a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and for inactivating the reset signal after a predetermined period following the initial supply to terminate an initialization of the internal circuit; and

a timing changing circuit for adjusting the predetermined period in accordance with an internal signal generated by ~~in an interior of~~ said timing changing circuit at the time of the initial supply.

2. (Previously Presented) The semiconductor integrated circuit according to claim 1, wherein said timing changing circuit changes an inactivation timing of the reset signal in accordance with said internal signal to be set at a predetermined logic level after the initial supply.

3. (Currently Amended) A ~~The~~ semiconductor integrated circuit ~~according to claim 1, further comprising~~ comprising:

a power-on resetting circuit for activating a reset signal in response to an initial supply of a power supply to initialize an internal circuit, and for inactivating the reset signal after a predetermined period following the initial supply to terminate an initialization of the internal circuit;

a timing changing circuit for adjusting the predetermined period in accordance with an internal signal generated in an interior of said timing changing circuit; and

a voltage generator for generating an internal supply voltage in accordance with an external supply voltage, ~~and~~ wherein

said timing changing circuit changes an inactivation timing of the reset signal in accordance with the internal signal corresponding to said internal supply voltage.

4. (Original) The semiconductor integrated circuit according to claim 3, wherein said timing changing circuit comprises a programming circuit having a fuse for changing said inactivation timing by programming the fuse corresponding to a level of said internal supply voltage.

5. (Original) The semiconductor integrated circuit according to claim 4, further comprising a testing circuit for changing said internal supply voltage to determine said fuse to be programmed for the sake of optimizing said inactivation timing.

6. (Original) The semiconductor integrated circuit according to claim 4, wherein said internal supply voltage is adjusted to a predetermined value simultaneously with the change of said inactivation timing, by programming said fuse.

7. (Previously Presented) A semiconductor integrated circuit comprising:

a power-on resetting circuit configured to inactivate a reset signal which initializes an internal circuit in response to a power supply being switched on, said inactivating performed in a predetermined period after activating the reset signal, and length of the predetermined period being controlled by a first adjusting signal;

a voltage generator configured to receive an external power supply voltage for generating an internal supply voltage, the level of the internal supply voltage being controlled by a second adjusting signal;

a programming circuit configured to output said first adjusting signal and said second adjusting signal; and

a signal selection circuit configured to receive an external signal, and to receive an external signal, and to receive said second adjusting signal from said programming circuit, to output the external signal to said voltage generator as said second adjusting signal in response to a test mode signal.

8. (Previously Presented) The semiconductor integrated circuit according to claim 7, wherein said signal selection circuit includes a mask circuit for masking an output from said programming circuit and for outputting said external signal as said second adjusting signal, in response to said test mode signal which is activated during a testing mode.

9. (Previously Presented) The semiconductor integrated circuit according to claim 7, wherein said programming circuit includes fuses configured to program the logical values of said first adjusting signal and said second adjusting signal.

10. (Previously Presented) The semiconductor integrated circuit according to claims 3, wherein said power-on resetting circuit and said voltage generator include transistors formed through a same manufacturing process.

11. (Previously Presented) The semiconductor integrated circuit according to claim 10, wherein said transistors are nMOS transistors that have same threshold voltages.

12. (Previously Presented) The semiconductor integrated circuit according to claims 7, wherein said power-on resetting circuit and said voltage generator include transistors formed through a same manufacturing process.

13. (Previously Presented) The semiconductor integrated circuit according to claim 12, wherein said transistors are nMOS transistors that have same threshold voltages.